CLAIMS

What is claimed is:

1. A FLASH array comprising:

a plurality of FLASH cells, each FLASH cell comprising a three-dimensional layout structure where sidewall, top and bottom surfaces of a floating gate include insulating and conducting films such that electrical parameters of an element of the FLASH cell can be accurately modeled and controlled.

2. The FLASH cell of claim 1 wherein the associated capacitive coupling factors are modeled accurately between a control gate, a floating gate and the conducting films.

3. The FLASH cell of claim 2 wherein the charge storage may be quantized by multiple threshold levels.

4. The FLASH cell of claim 2 wherein the physical layout of electrodes are based on proximity effects for the dimensional and shape customizations.

5. The FLASH cell of claim 2 wherein the proximity effects provide for the balanced control-to-floating-gate to bit-line-to-floating-gate capacitance ratios for all cell operation modes.

6. The FLASH cell of claim 2 wherein the proximity effects lead to lower voltage array operations, power, delay, and stressing advantages.

7. The FLASH cell of claim 2 wherein the proximity effects result in array compact sizes.

8. The FLASH cell of claim 2 wherein the proximity effects provide for device yield and cost advantages.

9. The FLASH arrays of claim 1 which includes a SCL circuit for low power logic peripherals and controls.

10. The FLASH arrays of claim 1 which include SCL peripheral circuitry that utilize 4T SRAMs.

11. The FLASH cell of claim 2 which includes SCL peripheral circuitry to form PLD/FPGA.

12. The FLASH cell of claim 2 which includes SCL peripheral circuitry to provide for use with hardwired or software macros.

13. A method of fabricating a FLASH cell comprising the steps of:

forming a plurality of a shallow trenches in a substrate;

forming tunnel oxide film above trenches;

etching at least one gate profile in association with the desirable capacitance coupling ratios;

providing a bit line film and word line film in accordance with desirable capacitance coupling ratios.

14. The method of claim 13 providing the physical layout of electrodes based upon proximity effects for the dimensional and shape customizer.

15. The method of claim 13 wherein the proximity effects provide for the balanced control-to-floating-gate to bit-line-to-floating-gate capacitance ratios for all cell operation modes.

16. The method of claim 13 wherein the proximity effects lead to lower voltage array operations, power, delay, and stressing advantages.

17. The method of claim 13 wherein the proximity effects result in array compact sizes.

18. The method of claim 13 wherein the proximity effects provide for device yield and cost advantages.